LM3485
Hysteretic PFET Buck Controller

General Description
The LM3485 is a high efficiency PFET switching regulator controller that can be used to quickly and easily develop a small, low cost, switching buck regulator for a wide range of applications. The hysteretic control architecture provides for simple design without any control loop stability concerns using a wide variety of external components. The PFET architecture also allows for low component count as well as ultra-low dropout, 100% duty cycle operation. Another benefit is high efficiency operation at light loads without an increase in output ripple.

Current limit protection is provided by measuring the voltage across the PFET’s R DS(ON), thus eliminating the need for a sense resistor. The cycle-by-cycle current limit can be adjusted with a single resistor, ensuring safe operation over a range of output currents.

Features
- Easy to use control methodology
- No control loop compensation required
- 4.5V to 35V wide input range
- 1.242V to V IN adjustable output range
- High Efficiency 93%
- ±1.3% (±2% over temp) internal reference
- 100% duty cycle
- Maximum operating frequency > 1MHz
- Current limit protection
- MSOP-8

Applications
- Set-Top Box
- DSL/Cable Modem
- PC/IA
- Auto PC
- TFT Monitor
- Battery Powered Portable Applications
- Distributed Power Systems
- Always On Power

Typical Application Circuit
Connection Diagram

Top View

Connection Diagram

Package Marking and Ordering Information

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Package Type</th>
<th>Package Marking</th>
<th>Supplied As:</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3485MM</td>
<td>MSOP-8</td>
<td>S29B</td>
<td>1000 units on Tape and Reel</td>
</tr>
<tr>
<td>LM3485MMX</td>
<td>MSOP-8</td>
<td>S29B</td>
<td>3500 units on Tape and Reel</td>
</tr>
</tbody>
</table>

Pin Description

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISENSE</td>
<td>1</td>
<td>The current sense input pin. This pin should be connected to Drain node of the external PFET.</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>Signal ground.</td>
</tr>
<tr>
<td>NC</td>
<td>3</td>
<td>No connection.</td>
</tr>
<tr>
<td>FB</td>
<td>4</td>
<td>The feedback input. Connect the FB to a resistor voltage divider between the output and GND for an adjustable output voltage.</td>
</tr>
<tr>
<td>ADJ</td>
<td>5</td>
<td>Current limit threshold adjustment. It connects to an internal 5.5µA current source. A resistor is connected between this pin and the input Power Supply. The voltage across this resistor is compared with the ( V_{DS} ) of the external PFET to determine if an over-current condition has occurred.</td>
</tr>
<tr>
<td>PWR GND</td>
<td>6</td>
<td>Power ground.</td>
</tr>
<tr>
<td>PGATE</td>
<td>7</td>
<td>Gate Drive output for the external PFET. PGATE swings between ( V_{IN} ) and ( V_{IN} -5V ).</td>
</tr>
<tr>
<td>VIN</td>
<td>8</td>
<td>Power supply input pin.</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- VIN Voltage: −0.3V to 36V
- PGATE Voltage: −0.3V to 36V
- FB Voltage: −0.3V to 5V
- ISENSE Voltage: −1.0V to 36V
- ADJ Voltage: −0.3V to 36V
- Maximum Junction Temp.: 150˚C
- Power Dissipation: 417mW @ TA = 25˚C

ESD Susceptibility
- Human Body Model (Note 3): 2kV
- Lead Temperature
  - Vapor Phase (60 sec.): 215˚C
  - Infrared (15 sec.): 220˚C
- Storage Temperature: −65˚C to 150˚C

Operating Ratings (Note 1)
- Supply Voltage: 4.5V to 35V
- Operating Junction Temperature: −40˚C to +125˚C

Electrical Characteristics
Specifications in Standard type face are for TJ = 25˚C, and in bold type face apply over the full Operating Temperature Range (TJ = −40˚C to +125˚C). Unless otherwise specified, VIN = 12V, VISNS = VIN − 1V, and VADJ = VIN − 1.1V. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min (Note 4)</th>
<th>Typ (Note 5)</th>
<th>Max (Note 4)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>IO</td>
<td>Quiescent Current at ground pin</td>
<td>FB = 1.5V (Not Switching)</td>
<td>250</td>
<td>400</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>VF</td>
<td>Feedback Voltage</td>
<td></td>
<td>1.226</td>
<td>1.242</td>
<td>1.258</td>
<td>V</td>
</tr>
<tr>
<td>VHYST</td>
<td>Comparator Hysteresis</td>
<td></td>
<td>10</td>
<td>15</td>
<td>14</td>
<td>20</td>
</tr>
<tr>
<td>VCL(Note 7)</td>
<td>Current limit comparator trip voltage</td>
<td>RADJ = 20kΩ</td>
<td>110</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>VCL OFFSET</td>
<td>Current limit comparator offset</td>
<td>VFB = 1.5V</td>
<td>−20</td>
<td>0</td>
<td>+20</td>
<td>mV</td>
</tr>
<tr>
<td>ICL ADJ</td>
<td>Current limit ADJ current source</td>
<td>VFB = 1.5V</td>
<td>3.0</td>
<td>5.5</td>
<td>7.0</td>
<td>µA</td>
</tr>
<tr>
<td>TCL</td>
<td>Current limit one shot off time</td>
<td></td>
<td>6</td>
<td>9</td>
<td>14</td>
<td>µs</td>
</tr>
<tr>
<td>RPGA</td>
<td>Driver resistance</td>
<td>Source</td>
<td>ISOURE = 100mA</td>
<td>5.5</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sink</td>
<td>ISINK = 100mA</td>
<td>8.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IPGA</td>
<td>Driver Output current</td>
<td>Source</td>
<td>VIN = 7V, PGATE = 3.5V</td>
<td>0.44</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sink</td>
<td>VIN = 7V, PGATE = 3.5V</td>
<td>0.32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VPAGEMIN</td>
<td>Minimum driver voltage</td>
<td>VIN = 4.5V</td>
<td>VFB = 1.0V</td>
<td>IISNS = 100µA sink</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>IFB</td>
<td>FB pin Bias Current (Note 8)</td>
<td>VFB = 1.0V</td>
<td></td>
<td>300</td>
<td>750</td>
<td>nA</td>
</tr>
<tr>
<td>TCNMIN_NOR</td>
<td>Minimum on time in normal operation</td>
<td>VISNS = VADJ + 0.1V</td>
<td>Cload on OUT = 1000pF</td>
<td></td>
<td>100</td>
<td>ns</td>
</tr>
</tbody>
</table>
Electrical Characteristics (Continued)

Specifications in Standard type face are for $T_J = 25^\circ C$, and in **bold type face** apply over the full **Operating Temperature Range** ($T_J = -40^\circ C$ to $+125^\circ C$). Unless otherwise specified, $V_{IN} = 12V$, $V_{ISNS} = V_{IN} - 1V$, and $V_{ADJ} = V_{IN} - 1.1V$. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

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<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{ONMIN,CL}$</td>
<td>Minimum on time in current limit</td>
<td>$V_{ISNS} = V_{ADJ} + 0.1V$</td>
<td></td>
<td></td>
<td>175</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{FB} = 1.0V$ C load on</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT = 1000pF (Note 9)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$%V_{FB/\Delta V_{IN}}$</td>
<td>Feedback Voltage Line Regulation</td>
<td>$4.5 \leq V_{IN} \leq 35V$</td>
<td></td>
<td>0.010</td>
<td></td>
<td>%/V</td>
</tr>
</tbody>
</table>

**Note 1:** Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

**Note 2:** The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J,MAX}$, the junction-to-ambient thermal resistance, $\theta_{JA} = 240^\circ C/W$, and the ambient temperature, $T_A$. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P_{D,MAX} = (T_{J,MAX} - T_A)/\theta_{JA}.$$ Exceeding the maximum allowable power dissipation will cause excessive die temperature.

**Note 3:** The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

**Note 4:** All limits are guaranteed at room temperature (standard type face) and at **temperature extremes** (bold type face). All room temperature limits are 100% tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

**Note 5:** Typical numbers are at 25°C and represent the most likely norm.

**Note 6:** The $V_{FB}$ is the trip voltage at the FB pin when PGATE switches from high to low.

**Note 7:** $V_{CL} = I_{CL,ADJ} \times R_{ADJ}$

**Note 8:** Bias current flows out from the FB pin.

**Note 9:** A 1000pF capacitor is connected between $V_{IN}$ and PGATE.
Typical Performance Characteristics

Unless otherwise specified, $T_J = 25^\circ C$

**Quiescent Current vs Input Voltage (FB = 1.5V)**

**Feedback Voltage vs Temperature**

**Hysteresis Voltage vs Input Voltage**

**Hysteresis Voltage vs Temperature**

**Current Limit ADJ Current vs Temperature**

**Current Limit One Shot OFF Time vs. Temperature**
Typical Performance Characteristics

Unless otherwise specified, $T_J = 25^\circ C$ (Continued)

PGATE Voltage vs Input Voltage

Operating ON Time vs Output Load Current
$(V_{IN} = 4.5V)$

Efficiency vs Load Current
$(V_{OUT} = 3.3V, L = 6.8\mu H)$

Minimum ON Time vs. Temperature

Operating ON Time vs Output Load Current
$(V_{IN} = 12V)$

Efficiency vs Load Current
$(V_{OUT} = 3.3V, L = 22\mu H)$

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Typical Performance Characteristics

Unless otherwise specified, $T_J = 25^\circ C$ (Continued)

**Efficiency vs Load Current**

$(V_{OUT} = 5.0V, L = 22\mu H)$

- $V_{IN} = 12V$
- $V_{IN} = 24V$

**Continuous Mode Operation**

$(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 500mA, L = 22\mu H)$

- Inductor Current
- SW node Voltage
- Output Ripple Voltage

**Discontinuous Mode Operation**

$(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 50mA, L = 22\mu H)$

- Inductor Current
- SW node Voltage
- Output Ripple Voltage

**Operating Frequency vs Input Voltage**

$(V_{OUT} = 3.3V, I_{OUT} = 1A, C_{OUT(ESR)} = 80m\Omega, C_{FF} = 100pF)$

**Output Ripple Voltage vs Input Voltage**

$(V_{OUT} = 3.3V, I_{OUT} = 1A, C_{OUT(ESR)} = 80m\Omega, C_{FF} = 100pF)$
Typical Performance Characteristics

Unless otherwise specified, $T_J = 25^\circ C$ (Continued)

Operating Frequency vs Output Load Current
($L = 22\mu H, C_{OUT(ESR)} = 45m\Omega, C_{ff} = 100pF$)

Feed-Forward Capacitor (Cff) Effect
($V_{OUT} = 3.3V, L = 22\mu H, I_{OUT} = 500mA$)
Functional Description

Overview
The LM3485 is buck (step-down) DC-DC controller that uses a hysteretic control scheme. The comparator is designed with approximately 10mV of hysteresis. In response to the voltage at the FB pin, the gate drive (PGATE pin) turns the external PFET on or off. When the inductor current is too high, the current limit protection circuit engages and turns the PFET off for approximately 9µs.

Hysteretic control does not require an internal oscillator. Switching frequency depends on the external components and operating conditions. Operating frequency reduces at light loads resulting in excellent efficiency compared to other architectures.

2 external resistors can easily program the output voltage. The output can be set in a wide range from 1.242V (typical) to VIN.

Hysteretic Control Circuit
The LM3485 uses a comparator based voltage control loop. The feedback is compared to a 1.242V reference and a 10mV hysteresis is designed into the comparator to ensure noise free operation.

When the FB input to the comparator falls below the reference voltage, the output of the comparator moves to a low state. This results in the driver output, PGATE, pulling the gate of the PFET low and turning on the PFET. With the PFET on, the input supply charges Cout and supplies current to the load via the series path through the PFET and the inductor. Current through the Inductor ramps up linearly and the output voltage increases. As the FB voltage reaches the upper threshold, which is the internal reference voltage plus 10mV, the output of the comparator changes from low to high, and the PGATE responds by turning the PFET off. As the PFET turns off, the inductor voltage reverses, the catch diode turns on, and the current through the inductor ramps down. Then, as the output voltage reaches the internal reference voltage again, the next cycle starts.

The LM3485 operates in discontinuous conduction mode at light load current or continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the inductor starts at zero and ramps up to the peak, then ramps down to zero. Next cycle starts when the FB voltage reaches the internal voltage. Until then, the inductor current remains zero. Operating frequency is lower and switching losses reduce. In continuous conduction mode, current always flows through the inductor and never ramps down to zero.

The output voltage (V\text{OUT}) can be programmed by 2 external resistors. It can be calculated as follows:

\[
V_{\text{OUT}} = 1.242\left(\frac{R_1 + R_2}{R_2}\right)
\]

FIGURE 1. Hysteretic Window
Functional Description  (Continued)

The minimum output voltage ripple ($V_{OUT_{PP}}$) can be calculated in the same way.

$$V_{OUT_{PP}} = V_{HYST} \frac{(R_1 + R_2)}{R_2}$$

For example, with $V_{OUT}$ set to 3.3V, $V_{OUT_{PP}}$ is 26.6mV

$$V_{OUT_{PP}} = 0.01 \times \frac{(33K + 20K)}{20K} = 0.0266V$$

Operating frequency ($F$) is determined by knowing the input voltage, output voltage, inductor, $V_{HYST}$, ESR (Equivalent Series Resistance) of output capacitor, and the delay. It can be approximately calculated using the formula:

$$F = \frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT}) \times ESR}{(V_{HYST} \times \alpha \times L) + (V_{IN} \times delay \times ESR)}$$

where:

$\alpha$: ($R_1 + R_2$) / $R_2$

delay: It includes the LM3485 propagation delay time and the PFET delay time. The propagation delay is 90ns typically. (See the Propagation Delay curve below.)

Current Limit Operation

The LM3485 has a cycle-by-cycle current limit. Current limit is sensed across the $V_{DS}$ of the PFET or across an additional sense resistor. When current limit is activated, the LM3485 turns off the external PFET for a period of 9µs (typical). The current limit is adjusted by an external resistor, $R_{ADJ}$.

The current limit circuit is composed of the ISENSE comparator and the one-shot pulse generator. The positive input of the ISENSE comparator is the ADJ pin. An internal 5.5µA current sink creates a voltage across the external $R_{ADJ}$ resistor. This voltage is compared to the voltage across the PFET or sense resistor. The ADJ voltage can be calculated as follows:

$$V_{ADJ} = V_{IN} - (R_{ADJ} \times 3.0\mu A)$$

Where 3.0µA is the minimum $I_{CL-ADJ}$ value.

The negative input of the ISENSE comparator is the ISENSE pin that should be connected to the drain of the external PFET. The inductor current is determined by sensing the $V_{DS}$. It can be calculated as follows.

$$V_{ISENSE} = V_{IN} - (R_{DSON} \times I_{IND-PEAK}) = V_{IN} - V_{DS}$$

The current limit is activated when the voltage at the ADJ pin exceeds the voltage at the ISENSE pin. The ISENSE comparator triggers the 9µs one shot pulse generator forcing the driver to turn the PFET off. The driver turns the PFET back on after 9µs. If the current has not reduced below the set threshold, the cycle will repeat continuously.

A filter capacitor, $C_{ADJ}$, should be placed as shown in Figure 3. $C_{ADJ}$ filters unwanted noise so that the ISENSE comparator will not be accidentally triggered. A value of 100pF to 1nF is recommended in most applications. Higher values can be used to create a soft-start function (See Start Up section).

The current limit comparator has approximately 100ns of blanking time. This ensures that the PFET is fully on when the current is sensed. However, under extreme conditions such as cold temperature, some PFETS may not fully turn on within the blanking time. In this case, the current limit threshold must be increased. If the current limit function is used, the on time must be greater than 100ns. Under low duty cycle operation, the maximum operating frequency will be limited by this minimum on time.

During current limit operation, the output voltage will drop significantly as well as operating frequency. As the load current is reduced, the output will return to the programmed voltage. However, there is a current limit fold back phenomenon inherent in this current limit architecture. See Figure 4.
At high input voltages (>28V) increased undershoot at the switch node can cause an increase in the current limit threshold. To avoid this problem, a low Vf Schottky catch diode must be used (See Catch Diode Selection). Additionally, a resistor can be placed between the ISENSE pin and the switch node. Any value up to approximately 600Ω is recommended.

Start Up
The current limit circuit is active during start-up. During start-up the PFET will stay on until either the current limit or the feedback comparator is tripped. If the current limit comparator is tripped first then the fold back characteristic should be taken into account. Start-up into full load may require a higher current limit set point or the load must be applied after start-up. One problem with selecting a higher current limit is inrush current during start-up. Increasing the capacitance (C_ADJ) in parallel with R_ADJ results in soft-start. C_ADJ and R_ADJ create an RC time constant forcing current limit to activate at a lower current. The output voltage will ramp more slowly when using the soft-start functionality. There are example start-up plots for C_ADJ equal to 1nF and 10nF in the Typical Performance Characteristics. Lower values for C_ADJ will have little to no effect on soft-start.

External Sense Resistor
The V_DS of a PFET will tend to vary significantly over temperature. This will result in an equivalent variation in current limit. To improve current limit accuracy an external sense resistor can be connected from VIN to the source of the PFET, as shown in Figure 5.

![FIGURE 4. Current Limit Fold Back Phenomenon](image)

![FIGURE 5. Current Sensing by External Resistor](image)
Design Information

Hysteretic control is a simple control scheme. However, the operating frequency and other performance characteristics highly depend on external conditions and components. If either the inductance, output capacitance, ESR, \( V_{IN} \), or \( C_F \) is changed, there will be a change in the operating frequency and output ripple. The best approach is to determine what operating frequency is desirable in the application and then begin with the selection of the inductor and \( C_{OUT} \) ESR.

**Inductor Selection (L1)**

The important parameters for the inductor are the inductance and the current rating. The LM3485 operates over a wide frequency range and can use a wide range of inductance values. A good rule of thumb is to use the equations used for National’s Simple Switchers®. The equation for inductor ripple (\( \Delta i \)) as a function of output current (\( I_{OUT} \)) is:

- for \( I_{OUT} < 2.0 \)Amps
  \[ \Delta i \leq I_{OUT} \cdot 0.3686726 + I_{OUT} \cdot 0.3 \]
- for \( I_{OUT} > 2.0 \)Amps
  \[ \Delta i \leq I_{OUT} \cdot 0.3 \]

The inductance can be calculated based upon the desired operating frequency where:

\[
L = \frac{V_{IN} - V_{DS} - V_{OUT}}{\Delta i} \cdot D \cdot \frac{1}{f}
\]

And

\[
D = \frac{V_{OUT} + V_D}{V_{IN} \cdot V_{DS} + V_D}
\]

where \( D \) is the duty cycle, \( V_D \) is the diode forward voltage, and \( V_{DS} \) is the voltag drop across the PFET.

The inductor should be rated to the following:

\[
I_{PK} = (I_{OUT} + \Delta i/2)^*1.1
\]

\[
I_{RMS} = \sqrt{I_{OUT}^2 + \Delta i^2/3}
\]

The inductance value and the resulting ripple is one of the key parameters controlling operating frequency. The second is the ESR.

**Output Capacitor Selection (C_{OUT})**

The ESR of the output capacitor times the inductor ripple current is equal to the output ripple of the regulator. However, the \( V_{HYST} \) sets the first order value of this ripple. As ESR is increased with a given inductance, then operating frequency increases as well. If ESR is reduced then the operating frequency reduces.

The use of ceramic capacitors has become a common desire of many power supply designers. However, ceramic capacitors have a very low ESR resulting in a 90° phase shift of the output voltage ripple. This results in low operating frequency and increased output ripple. To fix this problem a low value resistor should be added in series with the ceramic output capacitor. Although counter intuitive, this combination of a ceramic capacitor and external series resistance provide highly accurate control over the output voltage ripple. The other types capacitor, such as Sanyo POS CAP and OS-CON, Panasonic SP CAP, Nichicon “NA” series, are also recommended and may be used without additional series resistance.

For all practical purposes, any type of output capacitor may be used with proper circuit verification.

**Input Capacitor Selection (C_{IN})**

A bypass capacitor is required between the input source and ground. It must be located near the source pin of the external PFET. The input capacitor prevents large voltage transients at the input and provides the instantaneous current when the PFET turns on.

The important parameters for the input capacitor are the voltage rating and the RMS current rating. Follow the manufacturer’s recommended voltage derating. For high input voltage application, low ESR electrolytic capacitor, the Nichicon “UD” series or the Panasonic “FK” series, is available. The RMS current in the input capacitor can be calculated.

\[
I_{RMS,CIN} = I_{OUT} \cdot \frac{(V_{OUT} \cdot (V_{IN} - V_{OUT}))^{1/2}}{V_{IN}}
\]

The input capacitor power dissipation can be calculated as follows.

\[
P_{D,CIN} = I_{RMS,CIN}^2 \cdot ESR_{CIN}
\]

The input capacitor must be able to handle the RMS current and the \( P_D \). Several input capacitors may be connected in parallel to handle large RMS currents. In some cases it may be much cheaper to use multiple electrolytic capacitors than a single low ESR, high performance capacitor such as OS-CON or Tantalum. The capacitance value should be selected such that the ripple voltage created by the charge and discharge of the capacitance is less than 10% of the total ripple across the capacitor.

**Programming the Current Limit (R_{ADJ})**

The current limit is determined by connecting a resistor (\( R_{ADJ} \)) between input voltage and the ADJ pin.

\[
R_{ADJ} = I_{IND,PEAK} + R_{DSON} \cdot I_{CL,ADJ}
\]

where:

- \( R_{DSON} \) : Drain-Source ON resistance of the external PFET
- \( I_{CL,ADJ} \) : 3.0µA minimum
- \( I_{IND,PEAK} \) : \( I_{LOAD} + I_{RIPPLE}/2 \)

Using the minimum value for \( I_{CL,ADJ} \) (3.0µA) ensures that the current limit threshold will be set higher than the peak inductor current.

The \( R_{ADJ} \) value must be selected to ensure that the voltage at the ADJ pin does not fall below 3.5V. With this in mind, \( R_{ADJ,MAX} = (V_{IN} - 3.5)/7\mu A \). If a larger \( R_{ADJ} \) value is needed to set the desired current limit, either use a PFET with a lower \( R_{DSON} \) or use a current sense resistor as shown in Figure 5.

The current limit function can be disabled by connecting the ADJ pin to ground and ISENSE to VIN.

**Catch Diode Selection (D1)**

The important parameters for the catch diode are the peak current, the peak reverse voltage, and the average power dissipation. The average current through the diode can be calculated as following.
Design Information  (Continued)

\[ I_{D,AVE} = I_{OUT} \cdot (1 - D) \]

The off state voltage across the catch diode is approximately equal to the input voltage. The peak reverse voltage rating must be greater than input voltage. In nearly all cases a Schottky diode is recommended. In low output voltage applications a low forward voltage provides improved efficiency. For high temperature applications, diode leakage current may become significant and require a higher reverse voltage rating to achieve acceptable performance.

P-Channel MOSFET Selection (Q1)

The important parameters for the PFET are the maximum Drain-Source voltage (\( V_{DS} \)), the on resistance (\( R_{DSON} \)), Current rating, and the input capacitance.

The voltage across the PFET when it is turned off is equal to the sum of the input voltage and the diode forward voltage. The \( V_{DS} \) must be selected to provide some margin beyond the input voltage.

PFET drain current, \( I_{D} \), must be rated higher than the peak inductor current, \( I_{IND-Peak} \).

PGATE swings the PFET’s gate from \( V_{IN} \) to \( V_{IN} - 5V \) when the input voltage is greater than 7V. At less than 7V input, the PGATE voltage swing is smaller. At 4.5V input the PGATE swings from \( V_{IN} \) to \( V_{IN} - 3.3V \). To insure that the PFET turns on completely, a low threshold PFET should be used when the input voltage is less than 7V.

However, PFET switching losses will increase as the VGS threshold decreases. Therefore, whenever possible, a high threshold PFET should be selected. Total power loss in the FET can be approximated using the following equation:

\[ P_{Dswitch} = R_{DSON} \cdot I_{OUT} \cdot V_{IN} \cdot (t_{on} + t_{off}) / 2 \]

where:

- \( t_{on} = \) FET turn on time
- \( t_{off} = \) FET turn off time

A value of 10ns to 20ns is typical for \( t_{on} \) and \( t_{off} \).

The \( R_{DSON} \) is used in determining the current limit resistor value, \( R_{ADJ} \). Note that the \( R_{DSON} \) has a positive temperature coefficient. At 100°C, the \( R_{DSON} \) may be as much as 150% higher than the 25°C value. This increase in \( R_{DSON} \) must be considered when determining \( R_{ADJ} \) in wide temperature range applications. If the current limit is set based upon 25°C ratings, then false current limiting can occur at high temperature.

Keeping the gate capacitance below 2000pF is recommended to keep switching losses and transition times low. As gate capacitance increases, operating frequency should be reduced and as gate capacitance decreases operating frequency can be increased.

PCB Layout

The PC board layout is very important in all switching regulator designs. Poor layout can cause switching noise into the feedback signal and general EMI problems. For minimal inductance, the wires indicated by heavy lines should be as wide and short as possible. Keep the ground pin of the input capacitor as close as possible to the anode of the diode. This path carries a large AC current. The switching node, the node with the diode cathode, inductor, and FET drain, should be kept short. This node is one of the main sources for radiated EMI since it is an AC voltage at the switching frequency. It is always good practice to use a ground plane in the design, particularly at high currents.

The two ground pins, PWR GND and GND, should be connected by as short a trace as possible; they can be connected underneath the device. These pins are resistively connected internally by approximately 50\( \Omega \). The ground pins should be tied to the ground plane, or to a large ground trace in close proximity to both the FB divider and COUT grounds. The gate pin of the external PFET should be located close to the PGATE pin. However, if a very small FET is used, a resistor may be required between PGATE and the gate of the FET to reduce high frequency ringing. Since this resistor will slow the PFET’s rise time, the current limit blanking time should be taken into consideration (see Current Limit Operation).

The feedback voltage signal line can be sensitive to noise. Avoid inductive coupling to the inductor or the switching node, by keeping the FB trace away from these areas.

![FIGURE 6. Typical PCB Layout Schematic (3.3V output)](image-url)
C1: \( C_{\text{IN}} \) 22\( \mu \)F/35V EEJL1VD226R (Panasonic)
C2: \( C_{\text{OUT}} \) 100\( \mu \)F/6.3V 6TPC100M (Sanyo)
C3: \( C_{\text{ADJ}} \) 1nF Ceramic Chip Capacitor
C4: \( C_{\text{FF}} \) 100pF Ceramic Chip Capacitor
D1: 1A/40V MBRS140T3 (On Semiconductor)
L1: 22\( \mu \)H QH66SN220M01L (Murata)
Q1: FDC5614P (Fairchild)
R1: 33K\( \Omega \) Chip Resistor
R2: 20K\( \Omega \) Chip Resistor
R3: \( R_{\text{ADJ}} \) 24K\( \Omega \) Chip Resistor

FIGURE 7. Typical PCB Layout (3.3V Output)
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